REMARKS

Claim Rejection – Double Patenting

Claim 1 stands rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,751,723.

A timely filed terminal disclaimer in compliance with 37 C.F.R. 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground. 37 C.F.R. 1.130(b).

A terminal disclaimer has been submitted to overcome the nonstatutory double patenting rejection.

Applicant respectfully submits that Claim 1 is currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Claim Rejection – 35 U.S.C. §103

Claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Meyer et al. (U.S. 5,896,414) in view of van der Wal et al. (U.S. 6,188,381).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Amended Claim 1 recites an integrated circuit comprising "an FPGA virtual component interface translator having inputs and outputs, said inputs connected to said field programmable gate array core, wherein said FPGA virtual component interface translator is configured to translate signals from a first protocol to a second protocol ... a microcontroller virtual component interface translator having input and outputs, said inputs connected to said microcontroller, wherein said microcontroller virtual component interface translator is configured to receive a signal from said FPGA core in said second protocol and translate said signal into a third protocol for said microcontroller ...."

Meyer does not disclose an integrated circuit comprising an FPGA virtual component interface translator configured to translate signals from a first protocol to a second protocol, or a microcontroller virtual component interface translator configured to receive a signal from an FPGA core in the second protocol and translate the signal into a third protocol for a microcontroller, as recited in Claim 1. Applicant cannot find, nor has Examiner cited, any portion of Meyer that describes these claim limitations.

Van der Wal also does not disclose an integrated circuit comprising an FPGA virtual component interface translator configured to translate signals from a first protocol to a second protocol, or a microcontroller virtual component interface translator configured to receive a signal from an FPGA core in the second protocol and translate the signal into a third protocol for a microcontroller, as recited in Claim 1. Applicant cannot find, nor has Examiner cited, any portion of van der Wal that describes these claim limitations.

Since neither Meyer nor van der Wal disclose an FPGA virtual component interface translator or a microcontroller virtual component interface translator configured as in Claim 1, their combination cannot teach them. Therefore, all elements of Claim 1 are *not* disclosed in the prior art.

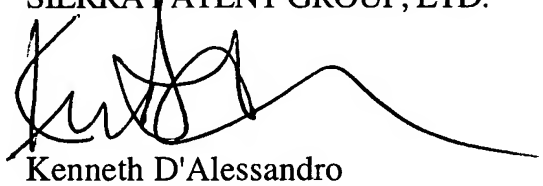
In the Notice of Allowance for the parent application (Serial No. 09/654,237) dated February 17, 2004, Examiner even admits that the prior art does not disclose "the FPGA translator for translating first protocol into a second protocol and the micro controller virtual component interface translator to receive signal from FPGA core in the second protocol and translating the signal into a third protocol for the micro controller, and the connection of the programmable routing resources in addition to the system bus."

Applicant respectfully submits that Claim 1 is patentable over Meyer in view of van der Wal. Therefore, Applicant respectfully submits that Claim 1 is currently in condition for allowance.

Reconsideration and withdrawal of the rejection is respectfully requested.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.



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